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Single-Phase Shift Modulation of DAB Converter in Typhoon HIL Simulation

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ABSTRACT — Solid-state transformer (SST) could be a solution for a future distribution system, in which many renewable energy sources (RES) are integrated. The SST consists of a single-phase dual-active bridge (DAB) converter, which is scale-down the dc voltage level. The control objective of the DAB converter used in the SST is to control its output voltage. This control strategy consists of a proportional-integral (PI) controller and a single-phase shift (SPS) modulation. Numerous literatures have mentioned about the SPS modulation for the DAB converter. However, they do not provide procedures in implementing the SPS modulation in the real controller. This paper aims to develop the SPS modulation in the real controller of the STM32F446RE microcontroller. The proposed SPS modulation is based on a master-slave timer feature, which is available in the STM32 microcontroller. The development process and testing of the complete control strategy of the DAB converter were carried out in the hardware-in-the-loop (HIL) simulation using Typhoon HIL. This scheme speeds up the development of process and reduces the costs. The experiment in the HIL environment shows that proposed control strategy of the DAB converter consisting of the PI controller and the SPS modulation is successfully implemented in the real microcontroller of the STM32F446RE. The proposed control strategy of the DAB converter is capable of bidirectional power flow, which is useful for integrating distributed generators in the load side. Moreover, this control strategy can reject the disturbance caused by loads.

KEYWORDS — DAB Converter, Typhoon HIL, PI Controller, SPS Modulation.

I. INTRODUCTION

A future distribution system will experience a reforming structure by existence of a solid-state transformer (SST) [1], [2]. It emerges due to advancement in power electronics field, especially power semiconductor devices that are the main components of the power converters [3]. This SST can replace a conventional bulky low-frequency transformer of 50 Hz, which cannot be controlled to compensate for disturbances in the distribution system [4]. Examples of disturbances are harmonics distortion, voltage sags, and voltage swells [5], [6]. This SST can also be used for fast-charging converters of electric vehicles [7]. The feature of bidirectional power flow of the SST enables vehicle-to-grid (V2G) or grid-to-vehicle (G2V) applications [8]. In addition, more and more renewable energy resources, such as photovoltaics and wind turbines, can be integrated easily into the grid through the SST [9].

The mentioned features of the SST are possible due to the flexibility in controlling voltage and current. It contrasts with the low-frequency transformer of 50 Hz that acts passively to the disturbances. Thus, voltage sag/swell can occur at the grid. The integration of the renewable energy sources is enabled by medium voltage dc (MVDC) or low voltage dc (LVDC) ports of the SST [10]. The bidirectional power flow is enabled by implementing a control strategy. Compared to a conventional transformer of 50 Hz, the overall dimension of the SST is smaller [11].

SST comprises three converters, namely a rectifier, a dc-dc converter, and an inverter [12], [13], as shown in Figure 1. This structure is called a three-stage SST, which provides both MVDC and LVDC ports [10]. Each converter has its own function. The rectifier converts MVAC into MVDC. This MVDC is scaled down to LVDC by the dc-dc converter. LVDC is converted to LVAC by the inverter. As a system, this SST is ac-to-ac conversion, which is flexibly controlled [14].

In this work, the dc-dc converter topology used is a single-phase dual-active bridge (DAB) converter. The conversion result can be higher or lower depending on its application. The DAB converter has superiority such as in high efficiency, galvanic isolation, and bidirectional power flow [15]. These features make the DAB converter a suitable option for the SST.

The considered architecture of the DAB converter is a modular structure, which several submodules are connected [16]. This architecture is suitable for adapting voltage levels. In the SST application, the DAB converter steps down the input voltage. Thus, a series-parallel connection of submodule DAB converters is utilized to step down the input voltage [17]. The transformation ratio of the submodule dc-dc converters could be a unity transformation. It refers to the condition where voltages of the DAB converter at both sides are the same. In a unity transformation, the DAB converter is more efficient because it naturally can achieve soft-switching capability in a light load and a heavy load [18].

Dimensions and mass of the passive components used in a DAB converter, such as capacitors and a transformer, can be smaller by increasing switching frequencies of the semiconductor devices. Thus, overall size of the DAB converter is smaller. However, the converter is less efficient when it is operated in a higher switching frequency [19]. For silicon insulated-gate bipolar transistors (Si IGBT) of 1,700 V, the switching frequency cannot be higher than 5 kHz due to the excessive heat that results in a high junction temperature [20]. This voltage class of the 1,700 V Si IGBT was used in this research.

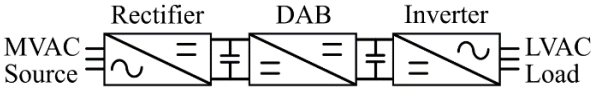

Figure 1. Solid-state transformer (SST) composed of three converters.

The control objective of the DAB converter used in the SST is to regulate the output voltage [21], [22]. Meanwhile, the input voltage of the DAB converter is regulated by the rectifier [23]. The typical control strategy of the DAB converter consists of a proportional-integrator (PI) controller and a single-phase-shift (SPS) modulation. The SPS modulation is a basic modulation technique to operate semiconductor devices of the DAB converter [24], [25]. This modulation performs well when voltage transformation ratio is unity [26]. Otherwise, other modulation techniques could be used as provided in literature [27]–[31]. In this research, the DAB converter for the SST application worked in a unity voltage transformation. Therefore, this converter worked using the SPS modulation.

The concept of the SPS modulation can be found in numerous pieces of literature. In reference [25], the SPS modulation was compared with other modulation techniques in terms of converter's efficiency and bidirectional power flow. This evaluation of the SPS modulation was carried out in a full simulation using PLECS software. In reference [32], the SPS modulation was improved by allowing a phase shift between legs of the DAB converter. It is intended to increase converter's efficiency. The improved SPS modulation was tested in a real hardware. However, it is unknown how to generate the SPS modulation in a real microcontroller. In reference [33], the SPS modulation was evaluated in a hardware-in-the-loop (HIL) simulation using OPAL-RT, which is useful to verify the control algorithm without risking real components. The SPS modulation was ran in a real controller. However, the realization of the SPS modulation in the real controller is unknown. In reference [34], the SPS modulation of the DAB converter for bidirectional EV chargers was tested in Typhoon HIL. The SPS modulation was implemented using STM32F4 microcontroller. However, there was no information how the SPS modulation was implemented the STM32F4 microcontroller.

This paper aims to provide a method in implementing the SPS modulation in the real controller of the STM32F446RE. The generation of the SPS modulation is based on a master-slave timer feature, which is available in the STM32 microcontroller. The SPS modulation is developed to capable of bidirectional power flow. It means the phase shift angle of the SPS modulation can be positive or negative depending on the power flow direction. This bidirectional power flow of the DAB converter enables distributed generators that are located near the loads can be connected into the grids [23]. Since this DAB converter is a part of the SST, the SPS modulation is integrated with the PI controller. Hence, this DAB converter can regulate its output voltage. This complete control strategy can reject the disturbances caused by loads or power injections. The verification of the proposed control strategy of the DAB converter is carried out in the HIL simulation, which is similar to reference [33]. However, in this research, a different HIL platform namely Typhoon HIL was utilized. This Typhoon HIL platform used for validating the SPS modulation is the same as reference [34]. But, in this paper, the implementation of the SPS modulation in a microcontroller is explained. This HIL simulation provides a quick, adaptable, and reliable method to validate experiments [34]. The HIL simulation also gives good accuracy [35]. In this HIL simulation scheme, the power stage was modeled in Typhoon HIL desktop app. Meanwhile, the control strategy was implemented in the real controller of the STM32F446RE.

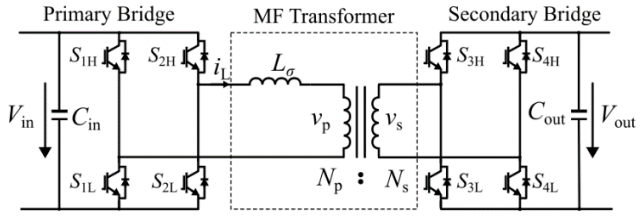

Figure 2. Circuit of a single-phase dual-active bridge converter.

This paper is arranged as follows. First, the modeling and control strategy of the single-phase DAB converter are discussed. Second, the concept of the HIL simulation is provided to give the overview related to the procedure for testing the real microcontroller. Third, this paper explains how the control method is executed on the STM32F446RE. The flowchart of the complete control strategy of the DAB converter for the SST is also provided. Next, the experiment results are discussed. Finally, the conclusion is provided to summarize the findings.

II. MODELING AND CONTROL STRATEGY

A. MODELING OF SINGLE-PHASE DAB CONVERTER

Figure 2 illustrates a single-phase DAB converter composed of two full-bridge converters [36]. The full-bridge converters are called primary and secondary bridges. These bridges are interconnected by a leakage inductance L_σ of a medium-frequency (MF) transformer. This converter has intrinsic a soft-switching capability [37]. Thus, it has high efficiency. In addition, this converter can accommodate power flow in both directions [38].

Shifting the secondary voltage v_s of the MF transformer allows for power to be transmitted from the input to the output side or from the output to the input side, as depicted in Figure 3. The phase angle φ between input and output voltages of the MF transformer determines the amount of transferred power. This phase shift can be controlled by utilizing an SPS modulation [26]. The performance of the SPS modulation is reasonably good when the transformation ratio is unity [26].

The dynamic of the transformer current i_L is [39]

$$\frac{di_L}{dt} = \frac{v_p - v_s}{L_\sigma}, \quad (1)$$

where v_p and v_s denote input and output voltages of the MF transformer, respectively. Figure 3 illustrates the typical transformer ac current waveform i_L under unity transformation. This ac current is drawn based on (1).

The power P transferred by the DAB converter is expressed as follows [40], [41]

$$P = \frac{nV_{in}V_{out}\varphi(\pi - |\varphi|)}{2\pi^2 f_{sw} L_\sigma}, \quad -\frac{\pi}{2} < \varphi < \frac{\pi}{2}, \quad (2)$$

where n is the transformation ratio, V_{out} is the output voltage, φ is the phase shift or the load angle, V_{in} is the input voltage, L_σ is the leakage inductance of the MF transformer, and f_{sw} is the switching frequency. Notice that the phase shift could be positive or negative. The positive phase shift means the power delivered from the DAB converter to the load, while the negative sign indicates the DAB converter absorbs the power.

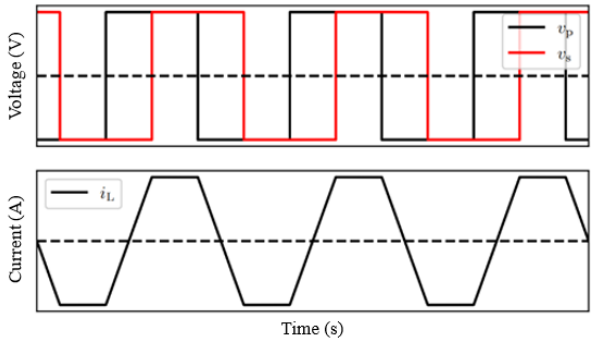

Figure 3. Typical waveforms of single-phase DAB converter under unity transformation ratio.

In other words, the sign of the phase shift angle determines the direction of the power flow. Based on (2), the maximum phase shift is ± 90°. It corresponds to the maximum load or maximum injected power.

By rearranging (2), the phase shift φ is obtained as [42]

$$\frac{\varphi}{\pi} = \frac{1}{2} - \sqrt{\frac{1}{4} - \frac{2I_{\text{out}}L_{\sigma}f_{\text{sw}}}{nV_{\text{out}}}} \quad (3)$$

where I_{out} is the output of the dc current. The dynamic characteristics of the DAB converter can be improved by incorporating a feedforward control, which uses (3) to calculate a required phase angle [43].

The leakage inductance L_{σ} comes from the MF transformer, but it can be also added externally [44]. The required leakage inductance L_{σ} can be derived from (2) by plugging $\varphi = 90^{\circ}$. This angle represents the maximum power. It yields [45]

$$L_{\sigma} = \frac{V_{\text{in}}V_{\text{out}}}{8nf_{\text{sw}}P}. \quad (4)$$

Using (4), the leakage inductance L_{σ} of the transformer will limit the transferred power. The maximum power occurs at the phase shift of 90°. However, it is not necessary to design the maximum power at the maximum angle of 90°. The desired power still can be achieved by setting the phase angle φ below then 90°, as long as (2) is obeyed. The choice of the phase shift angle φ will affect the value of the leakage inductance L_{σ} of the transformer. This selected leakage inductance L_{σ} can influence the current stress of the switching devices. It can be further optimized as explained in [46].

B. CONTROL STRUCTURE OF SINGLE-PHASE DAB CONVERTER

A DAB converter as a part of the SST controls its output voltage. Meanwhile, its input voltage is controlled by the rectifier as depicted in Figure 4. The voltage controller structure of this converter is shown in Figure 5 [47]. It consists of a PI controller and an SPS modulation.

For determining the gains of PI controller, an open-loop transfer function G_{ol} given in (5) is derived according to the control block diagram depicted in Figure 6.

$$G_{\text{ol}} = G_{\text{c}}G_{\text{p}}\, e^{-sT_{\text{d}}}. \quad (5)$$

The transfer function of the voltage regulator presented in (6) is denoted as G_{c}. The plant is modeled as G_{p} given in (7) [48]. This open loop model G_{ol} has a delay term $e^{-sT_{\text{d}}}$. It is added to represent a delay time, which is caused by a sample and hold of the digital implementation in a microcontroller [49].

$$G_{\text{c}} = K_{\text{p}} + \frac{K_{\text{i}}}{s}. \quad (6)$$

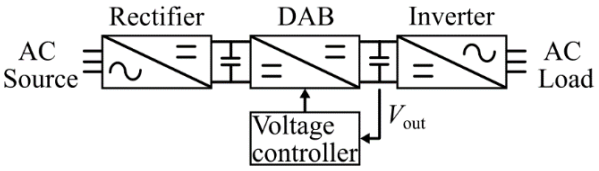

Figure 4. Control strategy of a solid-state transformer.

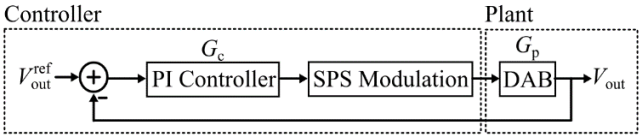

Figure 5. Voltage controller structure of a DAB converter.

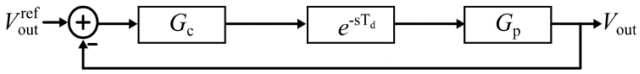

Figure 6. Control block diagram of a DAB converter.

$$G_{\text{p}} = \frac{1}{sC_{\text{out}}}. \quad (7)$$

Using the G_{ol}, the gains of PI controller are easily computed analytically or using a built-in function in MATLAB. The phase margin (PM) of 60° was selected as a control design specification.

III. HIL SIMULATION OF DAB CONVERTER AND IMPLEMENTATION OF SPS MODULATION

A. HIL SIMULATION OF DAB CONVERTER

HIL simulation is a tool to verify the performance of a control algorithm running on an actual controller [50], [51]. It can reduce risks of damages and speed up production. The HIL simulator can emulate the power circuit. The controller for the power stage comes from the real controller. The real controller sends and receives the signals from the HIL simulation as shown in Figure 7 [52]. Thus, a closed-loop system can be realized by this HIL simulation.

In this research, Typhoon HIL was used for the HIL simulator and STM32F446RE was used for the controller. The STM32F446RE is ARM Cortex M4 from STMicroelectronics. It has a clock rate of 180 MHz, three analog-to-digital converters (ADC) channels, various communication interfaces, and 14 timers [53].

The interface for connecting the controller to the Typhoon HIL Desktop App is Typhoon HIL 604. The power circuit of the DAB converter depicted in Figure 2 was modeled in Typhoon HIL Desktop App as shown in Figure 8.

Typhoon HIL 604 has 64 analog outputs and 64 digital inputs [54]. It is more than enough to test the controller of the single-phase DAB converter, which requires one analog output for the output voltage V_{out} and eight digital inputs for the PWM signals, as shown in Figure 8.

Typhoon HIL 604 and STM32F446RE have different voltage logic level. For Typhoon HIL 604, the voltage level of analog inputs and outputs is $\pm$ 10 V. For STM32F446RE, the voltage level is 3.3 V. Therefore, it requires scaling values in order to match as needed. The scaling values are easily configured in the Typhoon HIL Desktop App.

B. IMPLEMENTATION OF SPS MODULATION

A PI controller and an SPS modulation are the main control algorithm of the DAB converter. As mentioned before, the control objective of the DAB converter used in the SST is to

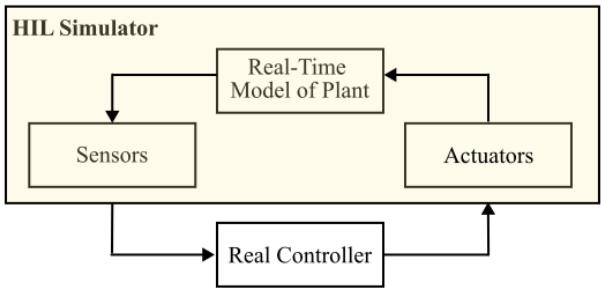

Figure 7. Diagram of a HIL simulation.

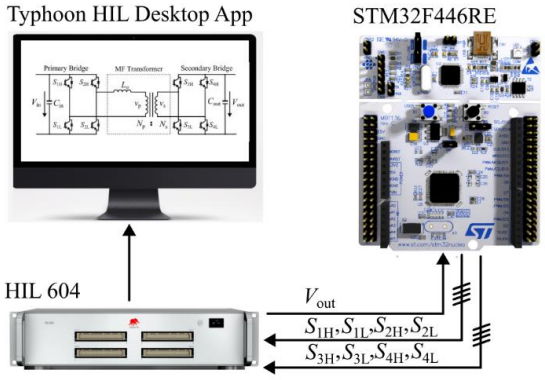

Figure 8. HIL simulation using Typhoon HIL and STM32F446RE microcontroller.

maintain the output voltage, regardless of the power direction. The power flows from the primary bridge to the secondary bridge of the DAB converter when delivering the power to the load. When the power is injected from the load side, the power flows from the secondary bridge to the primary bridge of the DAB converter. This feature is enabled by the SPS modulation that can shift the phase shift angle in both directions. In this subsection, the implementation of the SPS modulation in STM32F446RE will be explained. The implementation is based on the master-slave timer feature of the STM32F446RE microcontroller.

Prior to explaining the method of generating the SPS modulation, a working principle of the DAB converter is briefly explained. Each bridge of the DAB converter produces an ac square wave with a 50% duty cycle. In the case of the primary bridge shown in Figure 2, it can be achieved by turning on the switches S_{1H} and S_{2L} at the same time while keeping off the switches S_{1L} and S_{2H}. Similar procedures are applied to the secondary bridge, but the ac voltage of the secondary bridge is phase shifted in respect to the ac voltage produced by the primary bridge. The direction of the phase shift of the secondary bridge determines the power flow direction. Practically, this direction of the phase shift is associated with the sign of the phase shift angle, which can be a positive or negative angle. By phase shifting the ac voltage of the secondary bridge towards the primary bridge, power can be delivered through the circuit. It is due to a voltage difference between a leakage inductance of the medium frequency transformer.

For a bridge converter, the switches are categorized into high-side switches and low-side switches. In this research, the switches were labelled as S_{1H}, S_{2H}, S_{3H}, S_{4H} for the high-side switches and S_{1L}, S_{2L}, S_{3L}, S_{4L} for low-side switches. The low-side signals are complementary signals of the high-side signals.

In these complementary signals, a deadtime is commonly inserted to protect the real power-semiconductor switches [55].

The semiconductor switches in the Typhoon HIL is ideal switches. Theoretically, they do not need the deadtime. However, numerical errors occurred in the simulation. These errors are due to a deadtime violation (DTV) detection function, which is a built-in function in Typhoon HIL. The DTV forbids two switches in a half-bridge configuration to turn on at the same time. To resolve the error, an arbitrary number of the deadtime ($1\ \mu s$) was added so that the HIL simulation could be performed. Due to the complementary signals, the concern in PWM generation can be focused on the high-side switches.

To introduce a phase difference between the primary and the secondary bridges, all PWM signals of the secondary bridge were phase shifted with some amount of φ in respect to the primary bridge. This phase shift φ could be positive or negative depending on the power flow direction.

In STM32F446RE microcontroller, a PWM is obtained by comparing a counter register (*CNT*) value to *CCRx* value. The *CNT* is a register to store counting timer, while the *CCRx* is a duty cycle value. The variable *x* indicates the channel number. The maximum counting timer value determines the period of the PWM, which is stored in auto reload register (ARR), as shown in Figure 9 and Figure 10. In up-counting mode, the PWM signal can be active or inactive if the *CNT* is less than *CCRx*. In the example depicted in Figure 9(a) and Figure 9(b), the PWM signal is inactive when the CNT is less *CCRx*, which is half of the switching period or 50% of ARR. This configuration is called PWM mode 2.

The period value stored in *ARR* determines the switching frequency of the PWM signal. *ARR* is calculated as [56]

$$ARR = \frac{TIM\_CLK}{(PSC+1)\cdot f_{sw}} - 1 \qquad (8)$$

where *PSC* is 16-bit prescaler register, *TIM_CLK* is timer clock input, and f_{sw} is the desired switching frequency of the PWM signals. In default, the PSC is set to be zero. This value should be increased if the value of the *ARR* exceeds 16 bits.

Two kinds of timers of STM32F446RE were used for a master-slave timer. The master timer is a general-purpose timer, which does not have a complementary PWM output. However, this master timer can activate a trigger signal to trigger the slave timer. In this research, TIM2 and TIM4 were general-purpose timers. The slave timer is an advanced timer, which has more features compared to the general-purpose timer. It includes a deadtime between two complementary PWM signals. In this research, TIM1 and TIM8 were advanced timers. Each advanced timer of the STM32F446RE has three pairs of complementary PWM signals. In a single-phase of the DAB converter, two pairs of PWM signals are needed for each bridge of the converter.

Figure 9 shows the PWM generation concept for SPS modulation with a positive angle. The concept is by using a master-slave timer. When the master timer issues a trigger signal, the slave timer can start. The trigger signal occurs when the *CNT* value is the same with the *CCRx* value, as shown in Figure 9(a) and Figure 9(c). The trigger signal is named as internal trigger connection (ITR*x*). The master and slave timers are connected by ITR*x*, where x is the connection number. This connection is already specified by the manufacturer. In this research, the master timers were TIM2 and TIM4 and the slave timers were TIM1 and TIM8, as shown in Figure 9. TIM2 as a master and TIM1 as a slave was connected by ITR1. The master timer of TIM2 provided ITR1 to trigger TIM1. TIM1 generated four PWM signals for the primary bridge of the DAB converter.

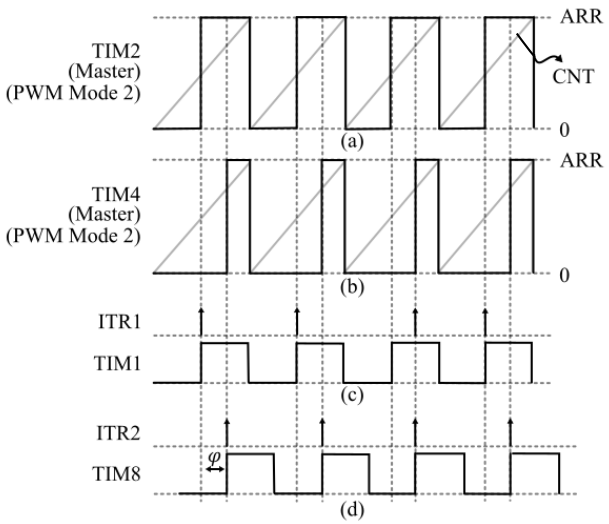

Figure 9. PWM generation concept for SPS modulation with a positive angle.

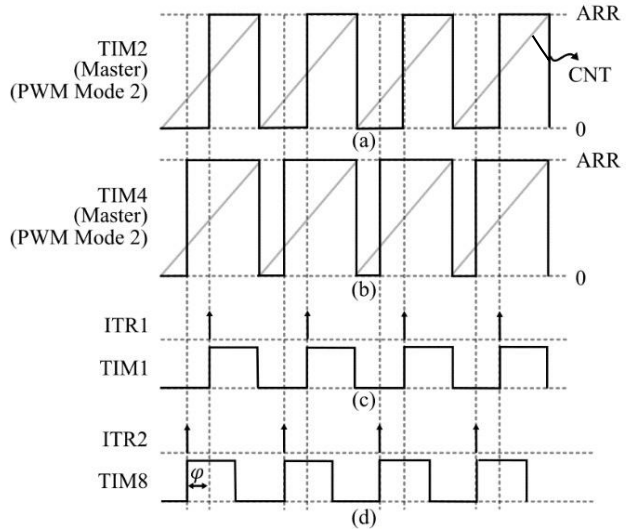

Figure 10. PWM generation concept for SPS modulation with a negative angle.

Similarly, TIM4 as a master and TIM8 as a slave was connected by ITR2. The master timer of TIM4 provided ITR2 to trigger TIM8. TIM8 generated four PWM signals for the secondary bridge of the DAB converter.

TIM2 and TIM1 are timers for generating PWM signals for the primary bridge of the DAB converter. As explained before, these PWM signals are stationary, which is a reference for the PWM signals of the secondary bridge. The TIM2 as a master timer was configured to run in PWM mode 2. It resulted in the PWM signal, as shown in Figure 9(a). The PWM signal turned high when the *CNT* matched the *CCRx* value, which is ½ *ARR*. It reset after reaching the ARR. At the time *CNT* matched with the *CCRx*, the ITR*x* was issued and triggered the TIM1. The PWM signals generated by TIM1 were predefined with a duty cycle of 50%. The TIM1 only waited to be triggered by ITR1, as shown in Figure 9(c).

TIM4 and TIM8 are timers for generating PWM signals for the secondary converter of the DAB converter. TIM4 is a master timer and TIM8 is a slave timer. The signals for the secondary bridge should be capable of phase shifting with a positive or negative angle. For the case of the positive angle, *CCRx* increases as formulated below

$$CCRx = \tfrac{1}{2}\,ARR + \varphi, \qquad \tfrac{1}{2}ARR \le \varphi \le \tfrac{3}{4}ARR. \qquad (9)$$

By increasing the value of *CCRx* of the TIM4 as formulated in (9), the duty cycle of the PWM signal of the TIM4 decreased. It is due to the PWM mode 2, which the PWM signal starts after the *CNT* matches with the *CCRx*. The rising edge of the PWM signal of the TIM4 issued the ITR2. This ITR2 started the TIM8 to generate the PWM mode 1 with the duty cycle of 50%. Using this method, the PWM signals of the TIM8 and the TIM1 were phase shifted for some amount of φ, as shown in Figure 9(c) and Figure 9(d). The PWM signals of the TIM8 were shifting to the right of the PWM signals of the TIM1, meaning that the power goes from the primary to the secondary sides.

The generation of the negative phase shift is similar to the generation of the positive phase shift. For the case of the negative angle, *CCRx* decreases as formulated below

$$CCRx = \tfrac{1}{2}\,ARR - \varphi, \qquad \tfrac{1}{4}ARR \le \varphi \le \tfrac{1}{2}ARR. \qquad (10)$$

The PWM signal of the TIM2 did not change, as shown in Figure 10(a). This is the same with the generation of the positive phase shift which is shown in Figure 9(a). Therefore, the generation of PWM signals of TIM1 are the same, as shown in Figure 10(c). The difference is the *CCRx* of the TIM4 was subtracted, as formulated in (10). This subtraction made the duty cycle of the PWM signal of the TIM4 larger, as shown in Figure 10(b). It is due to the PWM mode 2. The rising edge of the PWM signal of the TIM4 issued the ITR2. The ITR2 then triggered the TIM8 to start, as depicted in Figure 10(d). It made the PWM signals of the TIM8 shifted to the left. This shifting angle to the left is for power flow from the secondary to the primary sides.

The complete control strategy of the dual-active bridge converter covers the PI controller, and the single-phase shift modulation is explained in the flowchart shown in Figure 11. The program started by initializing the timer clock TIM_CLK, the prescaler PSC, and the desired switching frequency. Those parameters were used to calculate the ARR, which a register to store the period value. The calculation used (8). In this initialization, the timers of the microcontroller called TIM*x* were also configured. TIM2 and TIM4 were set to be master timers. Meanwhile, TIM1 and TIM8 were set to be slave timers. Each master timer only generated one signal PWM and one trigger signal ITR*x*. These generated signal PWMs of master timers were not connected to output pins of the microcontroller. They were just internal signals of the microcontroller. Each slave timer would be triggered by the ITR*x* generated by the corresponding master timer. Each slave timer would generate four PWM signals or two pairs of complementary signals with a deadtime. The duty cycle of the generated PWM signals was set to be 50%. Soon after the slave timers receive the trigger signal ITR*x*, they would generate the PWM signals with the duty cycle of 50%. After the parameter initialization, the register counter *CNT* was set to zero. In the next cycle, this *CNT* would count the value until reaching the value of ARR. After reaching it, the *CNT* would be reset. After setting the *CNT*, the program would compute an error. The error was obtained by subtracting the output voltage reference $V_{\text{out}}^{\text{ref}}$ and the output voltage V_{out} obtained from reading the voltage sensor. This error was then would be compensated by the PI controller. This PI controller would work to minimize the error so that the output voltage could come back to its reference, regardless of the loading or the injected power. The output of the PI controller was the required phase shift angle φ. The value of the phase shift could be positive or negative, depending on the

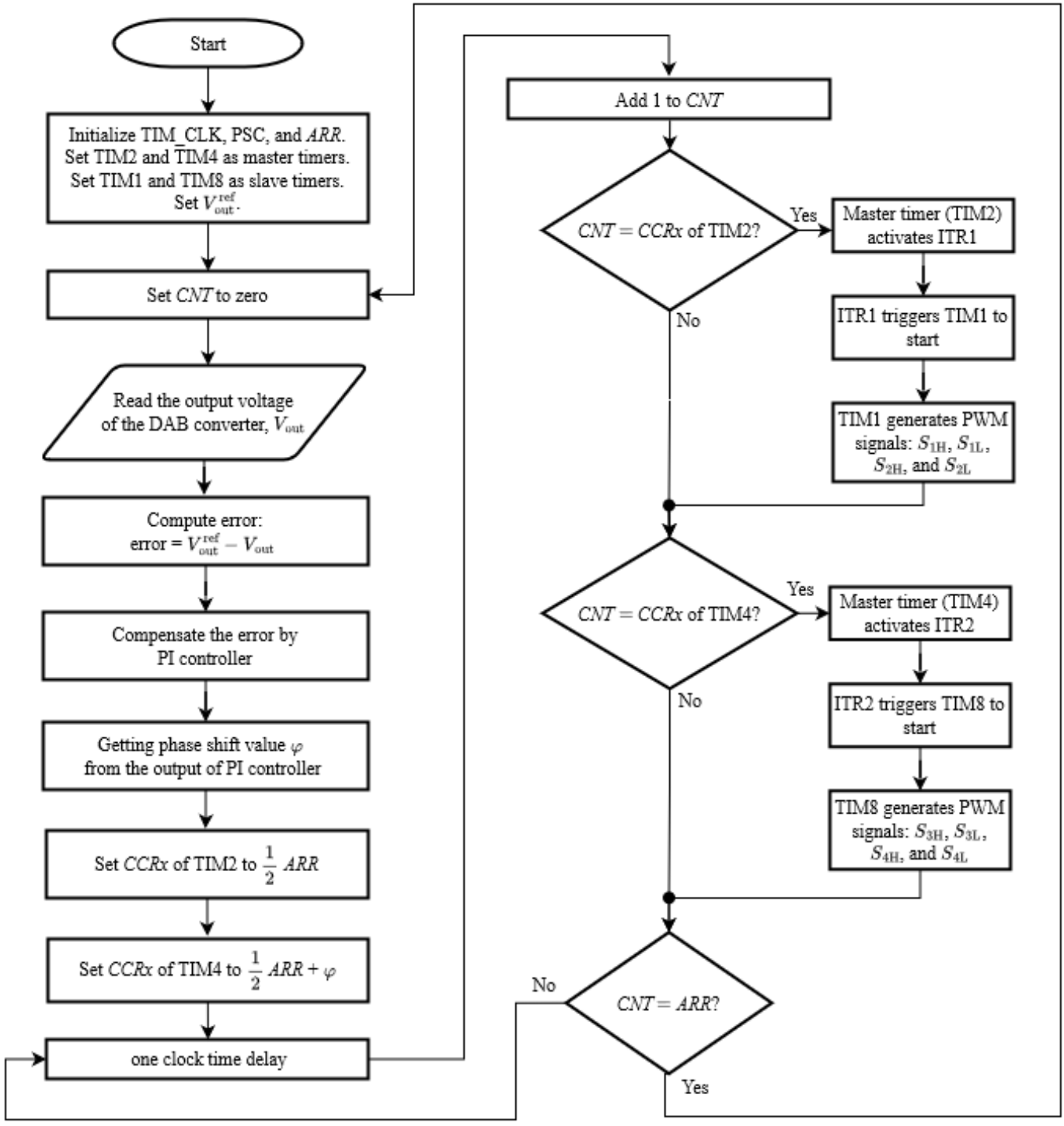

Figure 11. Flowchart of a controller strategy ofa dual-active bridge converter.

power flow direction as mentioned before. Next, the duty cycle register of the master timer TIM2 was set to ½ ARR. Meanwhile, the duty cycle register of the master timer TIM4 was set to ½ *ARR* + the phase shift angle φ. This scheme is according to (9) and (10). In the next step, if the counter register *CNT* matched with the duty cycle value of the TIM2, it would generate trigger signal ITR1. This ITR1 would trigger the slave timer TIM1 to start counting its timer and generate four PWM signals with duty cycles of 50%. In the next process, if the counter register *CNT* matched with the duty cycle value of the TIM4, it would generate trigger signal ITR2. This ITR2 would trigger the slave timer TIM8 to start counting its timer and generate four PWM signals with duty cycles of 50%. The counter timer register *CNT* would continue to count until reaching the maximum value of the *ARR*. Then, it would be reset to zero. The process worked continuously without stopping.

IV. RESULTS AND DISCUSSIONS

The test bench for the hardware-in-the-loop simulation based on the concept depicted in Figure 8 is shown in Figure 12. The STM32F446RE was connected to the HIL 604, which emulated the power circuit of the DAB converter depicted in Figure 2. The load of the DAB converter was modeled as a current source, which could be a positive or negative depending on the desired power flow. For measurements, signals coming

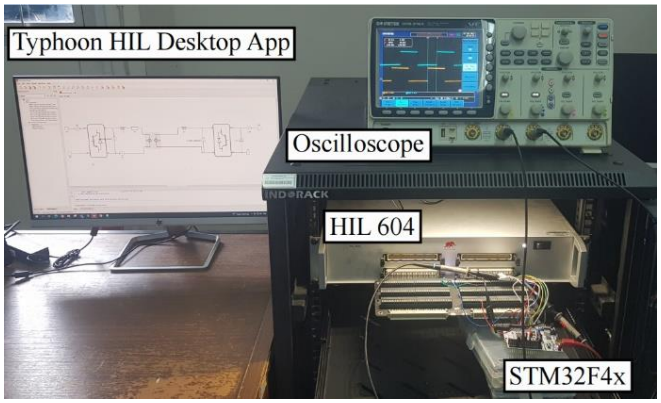

Figure 12. Testbench for hardware-in-the-loop simulation.

TABLE I
PARAMETERS OF DAB

Items	Descriptions	Value
P	Power rating	25 kW
V_{in}	Input voltage	1 kV
C_{in}	Input capacitance	1 mF
V_{out}	Output voltage	1 kV
C_{out}	Output capacitance	1 mF
f_{sw}	Switching frequency	5 kHz
L_{σ}	Leakage inductance	1 mH
I_{out}	Output current	-25 A to 25 A

in and out from STM32F446RE were observed using an oscilloscope. Other signals, especially signals in the power stage, were observed in a scope in Typhoon HIL. The signals were then exported as CSV files for the next process. The simulated parameters are listed in Table I.

A. SINGLE-PHASE SHIFT MODULATION

The method for generating the SPS modulation has been explained in Section IIIB. One bridge of the DAB converter requires four signals for operating semiconductor switches. In total, the DAB converter required eight PWM signals coming from the microcontroller STM32F446RE. The naming conventions of semiconductor switches are depicted in Figure 2. Each bridge of the DAB converter operated by the PWM signals resulted in square wave voltages, as shown in Figure 3. The amount of phase shift between these voltages determines the transferred power. Meanwhile, the sign of the phase shift determines the direction of the power. As explained in the Section I, the bidirectional power flow of the SST allowed the distributed generators at the load sides to transfer the power. It is the main advantage of the SST compared to the conventional transformer.

In observing the implemented SPS modulation, only two signals were needed. One signal from the primary bridge and one signal from the secondary bridge. In this experiment, the PWM signals of S_{1H} and S_{3H} were selected. S_{1H} is a PWM signal of the primary bridge and S_{3H} is a PWM signal of the secondary bridge, as depicted in Figure 2. Both signals were set as references for their related bridges. The phase difference between those signals determines the phase difference between input and output voltages of the MF transformer. In this case, the PWM signal S_{1H} was generated using a master timer. Thus, this signal was set for a reference of the S_{3H}. The PWM signal S_{3H} was generated by the slave timer that triggered by the master timer. The time for triggering the slave timer was the amount of the phase shift.

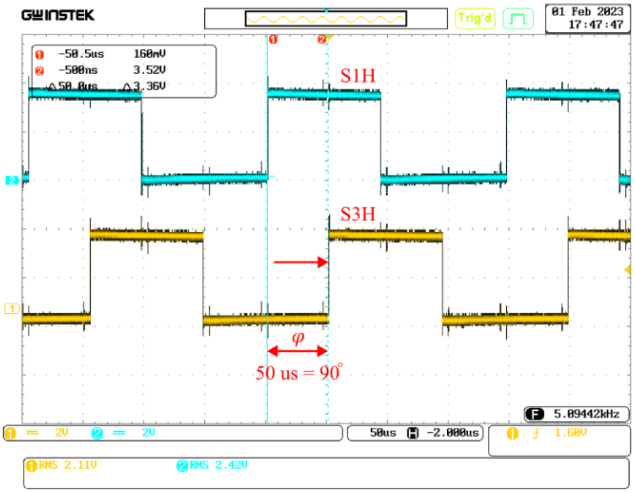

Figure 13. Positive phase shift angle of 90°.

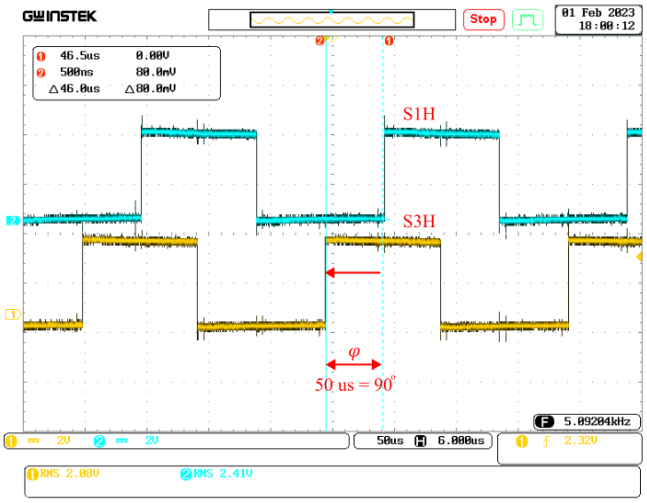

Figure 14. Negative phase shift angle of 90°.

Figure 13 shows the phase difference between S_{1H} and S_{3H}. The amount of the phase shift was 90°. This phase shift is due to the load of 25 A, which is the maximum load. The maximum load was corresponding to the 90° phase shift according to (2) [40]. In this case, the DAB converter supplied the power to the load. Figure 14 shows the controller response on the PWM signals of S_{1H} and S_{3H} when the load is -25 A, which is the maximum injected power. It shows that the S_{3H} shifted to the left, indicating that the DAB converter flowed the power from the output to the input sides of the DAB converter.

In summary, the single-phase-shift modulation was successfully implemented using the master-slave timer concept in STM32F446RE. Figure 13 and Figure 14 show that the implemented concept was capable for controlling the bidirectional power flow of the DAB converter.

B. PRIMARY CURRENT OF MF TRANSFORMER

In this part, the DAB converter modeled in Typhoon HIL was loaded with a resistor of 40 ohm. It represents the maximum load that can be connected to the DAB converter. The controller was from the real controller of STM32F446RE. The ac current of the MF transformer i_L was observed in the scope of the Typhoon HIL.

Figure 15 shows the ac current of the MF transformer at the input side. The waveform is the same as the typical waveform provided in Figure 3. It can be seen that the waveform is under

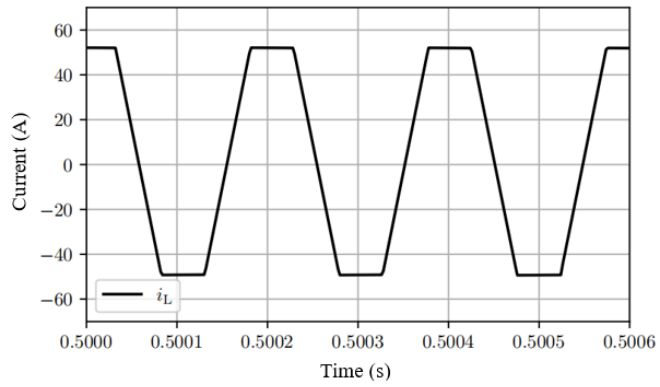

Figure 15. Primary current of MF transformer.

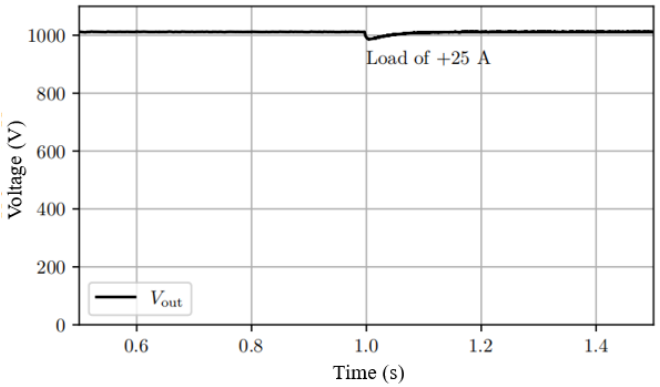

Figure 16. Output voltage V_{out} of the single-phase DAB converter.

a unity transformation ratio, which is indicated by the flat region on the top of the waveform. In the reality, under the unity transformation ratio, this region will be slightly decreased due to the losses.

C. VOLTAGE OF DAB CONVERTER

In this part, the output voltage control of the DAB converter shown in Figure 5 was examined. This controller includes the SPS modulation and the PI controller to regulate the output voltage of the DAB converter. The flowchart of the controller is shown in Figure 11. This control strategy was running on STM32F446RE, while the DAB converter was running on Typhoon HIL. This converter should maintain the output voltage V_{out} of 1000 V. Initially, the DAB converter has no load. It can be noticed in Figure 16 that the output voltage V_{out} is 1,000 V before connecting to the load at time before 1 s. At 1 s, the maximum load of 25 A is connected abruptly. This load disturbed the DAB converter. Thus, the output voltage V_{out} dropped due to this event. The controller of DAB converter implemented in STM32F446RE could bring back the output voltage V_{out} to 1,000 V. Based on the result above, it can be concluded that the controller strategy of the DAB converter implemented in STM32F446RE microcontroller is successfully tested in HIL environment. This HIL environment can speed up the development process of the controller because it can reduce the risk of damaging real semiconductor devices of the DAB converter during the development process of the controller.

V. CONCLUSION

This paper proposes a method in implementing an SPS modulation of the DAB converter in a real controller of the STM32F446RE. The method is based on master-slave timer feature that is available in the STM32 microcontroller. This SPS modulation was integrated with a PI controller to control the output voltage of the DAB converter. This complete control strategy is required by the DAB converter to function as part of the SST. The flowchart of the implemented control strategy is provided in this paper. The implemented control strategy was evaluated in the HIL simulation using Typhoon HIL. It provides an effective method in developing and testing the real controller of the STM32F446RE. The successful implementation of the proposed control strategy of the DAB converter in the real controller can be seen from the experiment results. The first result shows that the SPS modulation is capable of bidirectional power flow. In this scheme, the phase shift angle can be positive or negative depending on the power flow direction. The second result shows that the ac current transformer is the same as the typical ac current waveform of the DAB converter under unity transformation ratio. The third result shows that the control strategy can maintain the output voltage of the DAB converter. It can reject the disturbance caused by the abrupt change of the load. This paper also demonstrates the capability of the HIL simulation in verifying a control strategy without risking real components. Hence, the development of the control strategy can be more efficient.

CONFLICT OF INTEREST

The authors declare that his research was conducted and written without conflict of interest.

AUTHORS' CONTRIBUTION

Methodology, Yohan Fajar Sidik; software, Roni Irnawan; validation, F. Danang Wijaya; formal analysis, Yohan Fajar Sidik; investigation, Yohan Fajar Sidik, Muhammad Ridwan, Kevin Gausultan; data curation, Yohan Fajar Sidik; writing—original draft preparation, Yohan Fajar Sidik; visualization, Yohan Fajar Sidik; writing—review and editing, Yohan Fajar Sidik; supervision, F. Danang Wijaya, Sriyono.

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