

Design of Medium Power AC-DC Flyback LED Driver

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Abstrak

Pangsa pasar lampu LED menunjukkan tren yang semakin meningkat. Hal ini didorong oleh beberapa kelebihan yang dimiliki oleh lampu LED, seperti efisiensi yang lebih tinggi, banyak pilihan warna, dan masa pakai yang lebih lama. LED merupakan sebuah devais DC, dan untuk menyalakannya dari catu AC, seperti lampu rumah dan lampu jalan, diperlukan driver untuk mengubah listrik AC menjadi DC. Selain itu, driver LED biasanya beroperasi dalam mode arus konstan untuk mencegah kerusakan LED akibat panas berlebih. Driver LED juga harus memiliki efisiensi yang tinggi, THD yang rendah, dan memenuhi persyaratan emisi elektromagnetik. Dalam penelitian ini, telah dibuat sebuah prototipe driver LED AC-DC yang diregulasi pada sisi primer berdasarkan topologi flyback. Driver tersebut memiliki arus keluaran konstan $0.990A \pm 0.012A$ sepanjang rentang tegangan keluaran $15.59V - 42.80V$. Hasil pengukuran menunjukkan bahwa efisiensi tertinggi mencapai 88.55%, harmonisa arus memenuhi standar IEC 61000-3-2, dan tingkat conducted emission memenuhi persyaratan CISPR 15.

Kata kunci—regulasi sisi primer, driver LED, flyback, harmonisa, conducted emissions, EMC

Abstract

LED lighting market share shows an ever increasing trend. This is driven by some of the LED advantages, such as higher efficiency, wide range of colors, and longer lifetime. LED is a DC device, and to power it from AC supply, like in household or street lightings, a driver is required to convert AC to DC supply. In addition, LED driver is preferred to operate in constant current mode in order to avoid LED thermal runaway. Also the driver has to have high efficiency, low THD (total harmonic distortion), and comply with electromagnetic emission limits. In this paper, a prototype of primary-side-regulated AC-DC flyback LED driver has been implemented. It has a constant output current of $0.990A \pm 0.012A$ across the output voltage $15.59V - 42.80V$. Measurement results show that the achieved efficiency is up to 88.55%, current harmonics comply with IEC 61000-3-2, and conducted emission levels comply with CISPR 15.

Keywords—primary side regulated, LED driver, flyback, harmonics, conducted emissions, EMC

1. INTRODUCTION

Nowadays, the development of LED solid-state lighting has greatly increased since the discovery of blue LED based on InGaN by Nakamura et al which was announced at a press conference in 1993 [1]. LED is an electronic component that can emit light when given a constant current, and it is able to replace the conventional lamps such as incandescent and fluorescent lamps. LEDs have been widely used in various applications including household illumination, traffic signals, large outdoor displays, interior and exterior lighting in vehicles, backlighting for cellular phones and display panels, UV disinfection, and many more [2,3]. The utilization of LED as a light source due to its advantages, such as high energy efficiency, long lifetime, high reliability, low UV radiation, small size, and easy to control.

Besides having many advantages, LEDs also have disadvantages that it requires a steady flow of electric current to maintain the performance and constant temperature. In case the LEDs are overheating, they will be prone to malfunction. Therefore, the LED driver is required to manage the current supplied to the LED and also act as a protective barrier against power surges. For driving the LED we can use linear or switching regulators depending on the requirement.

When the ratio of supply voltage to output voltage is high, switching regulator is preferred because it can achieve higher efficiency. This kind of regulator regulates an output voltage with pulse width modulation (PWM). The higher efficiency can be achieved because of internally switching a transistor (or MOSFET) and it produces lower power dissipation. When the switching transistor is fully "ON" and conducting current, the voltage drop across it is at its minimal value, and when the transistor is fully "OFF" there is no current flow through it. Switching regulators can be configured in several basic topologies, such as buck, boost, buck-boost, and flyback. The main disadvantage of switching regulator is the high-frequency noise emission because of switching operation of MOSFET that produces electromagnetic interference (EMI) and usually requires EMI filter or RF shielding to prevent interference with other systems [4].

Flyback topology is broadly used because of its high efficiency, simple topology, electrical isolation, low cost, and compact volume. It is suitable for the development of low power offline applications such as LED power supplies with multiple output voltages. The flyback converter can operate in Discontinuous Conduction Mode (DCM), Boundary Conduction Mode (BCM), and Continuous Conduction Mode (CCM) [5,6,7].

In DCM, the single-stage flyback converter with Power Factor Correction can achieve unity power factor, however, the conduction loss, voltage stress, and current stress on the switch will significantly increase. The power factor correction can be achieved due to the linear relationship between the average input current and the input voltage. For high power applications, the CCM is preferably suggested to achieve higher efficiency and higher power factor, even though the control is more complex, and sometimes have poor stability [7]. Generally, LED lamp is operated with power lower than 100W. So, it is more appropriate to operate the power converter for driving LED lamp in BCM or DCM [8].

Flyback converter is an isolated converter, the output voltage and current are conventionally regulated by using the Secondary Side Regulation (SSR) which is particularly composed of an opto-coupler and a secondary error amplifier. By modulating the opto-coupler LED current, the regulation information is sent back to the primary-side controller, which adjusts the frequency and/or the primary peak current to keep the output voltage at its nominal value. Because of its high precision and fast response this method is widely used. However, there are several problems of using opto-couplers. It is relatively expensive and poses high requirements for the layout and volume of the driver. Furthermore, the opto-coupler has the frequency limit of 20-30kHz, which makes it impossible to be used in drivers that work in very high frequency [5,9]

Nowadays, Primary Side Regulation (PSR) flyback converter becomes an important technology, due to lower cost and standby power losses [9]. PSR consists of regulating the output current or the output voltage of the flyback by observing waveforms from the primary side of the converter. This method decreases the bill of materials of the flyback converter by removing the opto-coupler or the operational amplifier sensing the output voltage, and also can improve power stage life-time and reliability. The output current is estimated by sensing the current in the primary-side MOSFET. The output voltage is regulated by sensing the auxiliary winding voltage—the output voltage during the off-time of the power MOSFET. Furthermore, a distinct functional advantage of PSR derives from having an absolute measure of the output voltage. Primary-side Constant Current/Constant Voltage converters are generally operated in BCM or DCM, and rarely used in CCM, except for high power applications [10,11,12].

The objective of this research is to design a primary side regulated AC-DC Medium Power Flyback LED Driver that comply to EMI standard based on CISPR 15 and current harmonic distortion standard based on IEC 61000-3-2.

2. METHODS

2.1 Power Stage Design

The following table summarizes the design specifications:

Table 1. Design Specifications

Input voltage (V_{IN})	90 – 250 V _{AC}
Max output voltage ($V_{OUT.MAX}$)	45 V _{DC}
Constant output current (I_{OUT})	1 A
Maximum duty cycle	40%
Max switching frequency (f_s)	65 kHz
Expected efficiency (η)	88%
Core cross sectional area (A_e)	122 mm ²
Flyback controller	FL7733

In flyback converter, magnetizing inductance (L_m) is charged by directly applying input voltage (V_{IN}) during MOSFET turn-on (t_{ON}). Therefore, the MOSFET drain current (I_{DS}) peaks form a sinusoidal envelope resembling the input voltage, as shown in Figure 1 [13].

$$I_{DS}(\theta) = \frac{V_{IN.PK} \cdot |\sin(\theta)| \cdot t_{ON}}{L_m} \quad (1)$$

Consequently the AC input current (I_{IN}) drawn to charge L_m can be calculated as the area of triangular-shaped I_{DS} [14].

$$I_{IN}(\theta) = \frac{1}{2} \cdot \frac{t_{ON}}{t_S} \cdot I_{DS}(\theta) \quad (2)$$

$$= \frac{1}{2} \cdot \frac{t_{ON}}{t_S} \cdot \frac{V_{IN.PK} \cdot |\sin(\theta)| \cdot t_{ON}}{L_m} \quad (3)$$

$$I_{IN.PK} = \frac{1}{2} \cdot \frac{t_{ON}^2 \cdot V_{IN.PK}}{t_S \cdot L_m} \quad (4)$$

The drain current is continuously monitored by the FL7733 controller in order to avoid LED over current. It is sensed by measuring the voltage V_{CS} across the current sense resistor R_S . The maximum voltage $V_{CS.PK}$ is typically set as $0.85V$ [14]. Therefore,

$$\begin{aligned} V_{CS.PK} &= I_{DS.PK} \cdot R_S \\ 0.85 &= 4.01 \times R_S \\ R_S &= \mathbf{0.212\Omega} \end{aligned} \quad (11)$$

In a primary side regulation driver, the output current I_O is estimated from the transformer discharge time t_{DIS} and the peak drain current I_{DS} [13]. The I_O can be obtained by computing the area of the triangular-shaped transformer secondary discharge current as show in Figure 1 .

$$I_O = \frac{1}{2} \cdot \frac{t_{DIS}}{t_S} \cdot \frac{V_{CS}}{R_S} \cdot n_{PS} \quad (12)$$

Meanwhile, the FL7733A implements a control algorithm that satisfies the following condition:

$$\frac{t_{DIS}}{t_S} \cdot V_{CS} = 0.25 \quad (13)$$

From (12) and (13), I_O can be rewritten as:

$$I_O = 0.125 \cdot \frac{n_{PS}}{R_S} \quad (14)$$

From (14) transformer's primary to secondary ratio n_{PS} can be calculated:

$$\begin{aligned} 1 &= 0.125 \times \frac{n_{PS}}{0.212} \\ n_{PS} &= \mathbf{1.696} \end{aligned} \quad (15)$$

To avoid saturation of transformer core, a minimum number of turns should be determined. Minimum turns of primary coil can be computed as follows [15]:

$$N_p > \frac{V_{IN.MIN.PK} \cdot t_{ON.MAX}}{B_{SAT} \cdot A_E} \quad (16)$$

Given the typical saturation magnetic flux density of ferrite $B_{SAT}=0.22T$ and the core (PQ2620) cross sectional area $A_e = 122 \text{ mm}^2$, the minimum primary turns can be obtained as:

$$N_p > \frac{\sqrt{2} \times 90 \times 0.4}{0.22 \times 122 \times 10^{-6} \times 65 \times 10^3} > 29.18 \text{ turns} \approx \mathbf{30 \text{ turns}} \quad (17)$$

Therefore, from (15) number of secondary turns N_S can be determined:

$$1.696 = \frac{30}{N_S} \quad (18)$$

$$N_S = \mathbf{18 \text{ turns}}$$

LED output over voltage $V_{O.OVP}$ is set as $50V$, whereas the FL7733A over voltage protection is activated when $V_{DD} = 23V$. On the other hand, V_{DD} is supplied from the auxiliary coil voltage V_{AUX} during MOSFET turn-off time, which is coupled to the secondary coil. Thus, the auxiliary turns N_A can be obtained as:

$$n_{AS} = \frac{V_{DD.OVP}}{V_{O.OVP}} = \frac{N_A}{N_S} \quad (19)$$

$$= \frac{23}{50} = \frac{N_A}{18}$$

$$N_A = \mathbf{8 \text{ turns}}$$

where n_{AS} is the auxiliary to secondary turn ratio.

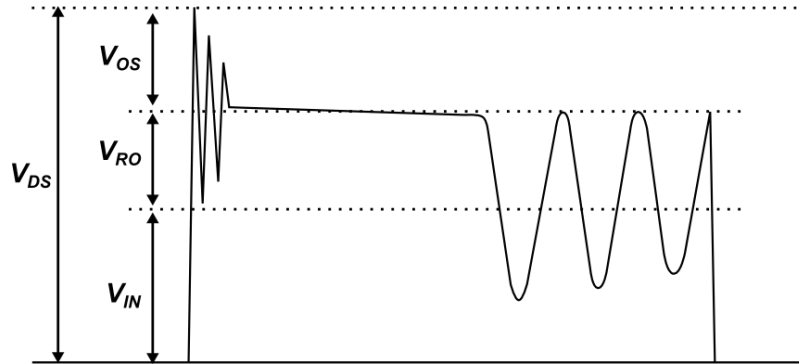


Figure 2. MOSFET drain voltage waveform

Referring to Figure 2, with overshoot voltage V_{OS} is estimated 100V, MOSFET maximum drain voltage $V_{DS.MAX}$ can obtained as:

$$V_{DS.MAX} = V_{IN.MAX.PK} + V_{RO} + V_{OS} \quad (20)$$

$$= V_{IN.MAX.PK} + n_{PS} \cdot (V_{O.OVP} + V_{F.DO}) + V_{OS}$$

$$= \sqrt{2} \times 250 + \frac{30}{18} \times (50 + 1) + 100$$

$$= \mathbf{538 \text{ volts}}$$

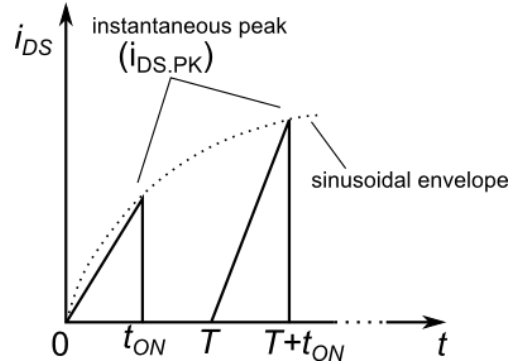


Figure 3. Conceptual waveform of the MOSFET drain current

Theoretically, the MOSFET instantaneous drain current peaks $i_{DS.PK}$ form a sinusoidal envelope. During each switching period T , the drain current ramps up for t_{ON} long such that it forms a triangular shape. Therefore, to calculate the average input current $I_{DS.RMS}$, first the average triangular current $I_{\Delta.RMS}$ is computed as follows:

$$I_{\Delta.RMS} = \sqrt{\frac{1}{T} \int_0^T i(t)^2 dt} \quad (21)$$

$$= \sqrt{\frac{1}{t_S} \int_0^{t_{ON}} \left(i_{DS.PK} \cdot \left(\frac{t}{t_{ON}} \right) \right)^2 dt} \quad (22)$$

$$= i_{DS.PK} \sqrt{\frac{1}{t_S} \cdot \left[\frac{1}{3} \cdot \frac{t^3}{t_{ON}} \right]_0^{t_{ON}}} \quad (23)$$

$$= i_{DS.PK} \sqrt{\frac{t_{ON}}{3 \cdot t_S}} \quad (24)$$

Then, the average input current $I_{DS.RMS}$ is obtained by computing the current root-mean-square over the mains half cycle. This is sufficient because the other half cycle is theoretically symmetrical.

$$I_{DS.RMS} = \sqrt{\frac{1}{\pi} \int_0^{\pi} (I_{\Delta.RMS.MAX} \cdot \sin(\theta))^2 d\theta} \quad (25)$$

$$= I_{\Delta.RMS.MAX} \sqrt{\frac{1}{\pi} \cdot \left[\frac{1}{2} (\theta - \sin(\theta) \cdot \cos(\theta)) \right]_0^{\pi}} \quad (26)$$

$$= I_{\Delta.RMS.MAX} \sqrt{\frac{1}{2\pi} \cdot (\pi - 0)} \quad (27)$$

$$= i_{DS.PK.MAX} \sqrt{\frac{t_{ON}}{6 \cdot t_S}} \quad (28)$$

$$= I_{DS.PK} \times \sqrt{\frac{0.4}{6}} \quad (29)$$

$$= 4.01 \times \sqrt{\frac{0.4}{6}} = \mathbf{1.035 A} \quad (30)$$

Maximum reverse voltage that occurs at the output diode $V_{D.MAX}$ can be calculated as follows:

$$V_{D.MAX} = V_{IN.MAX.PK} \cdot \frac{N_S}{N_P} + V_{O.MAX} \quad (31)$$

$$= \sqrt{2} \times 250 \times \frac{18}{30} + 50 = \mathbf{262 V} \quad (32)$$

Whereas the maximum peak current flowing in the output diode $I_{D.MAX}$ can be computed as follows:

$$I_{D.MAX} = I_{DS.PK} \times \frac{N_P}{N_S} \quad (33)$$

$$= 4.01 \times \frac{30}{18} = \mathbf{6.68 A} \quad (34)$$

In summary, the power stage design parameters are described in Table 2:

Table 2. Power stage design parameters

Sensing resistor	Current sense resistor	R_S	0.212 Ω
Transformer	Magnetizing inductance	L_m	194.95 μH
	Primary to secondary ratio	n_{PS}	1.696
	Number of primary winding	N_P	30 turns
	Number of secondary winding	N_S	18 turns
	Number of auxiliary winding	N_A	8 turns
Primary switch	Maximum peak drain current	$I_{DS.PK}$	4.01 A
	Maximum peak drain voltage	$V_{DS.MAX}$	538 V
	Average input current	$I_{DS.RMS}$	1.035 A
Secondary switch	Maximum reverse voltage	$V_{D.MAX}$	262 V
	Maximum peak current	$I_{D.MAX}$	6.68 A

MOSFET FCPF400N80 has been chosen as the primary switch, and it has the capability to deal with the current and voltage stress as calculated above. FCPF400N80 has a drain to source

breakdown voltage of 800 V and maximum drain current handling of 8.9 A at 100°C. Meanwhile, diode RHRP3060 functions as the secondary switch. It has a maximum reverse voltage of 600 V and maximum forward current of 30 A, which are sufficient to support the driver operation.

2.2. EMI Filter Design

Blue trace in Figure 8 shows the measured conducted emissions (CE) of the LED driver without EMI filter in place. The CE levels are clearly exceeding CISPR 15 limit. The fundamental switching frequency at 60 kHz peaks at around 115 dBuV. To suppress the amplitude below the limit line, let it be 80 dBuV, then 35 dB of attenuation is required. It is known that at fundamental switching frequency differential-mode (DM) noise is dominant. A DM filter based on single stage LC filter, whose attenuation of 40 dB/decade, is designed as follows. The filter cut-off frequency f_c is obtained as:

$$40 \cdot \log \frac{f_n}{f_c} = A_n \quad (35)$$

$$40 \cdot \log \frac{60 \text{ kHz}}{f_c} = 35 \text{ dB} \quad (36)$$

$$f_c = \mathbf{8 \text{ kHz}} \quad (37)$$

where f_n and A_n is the known frequency and required attenuation at that frequency. Given the inductors are a pair of 470 μH placed on both live and neutral lines, the capacitor can be calculated as follows:

$$f_c = \frac{1}{2\pi\sqrt{LC}} \quad (38)$$

$$8\text{kHz} = \frac{1}{2\pi\sqrt{2 \times 470 \text{ uH} \times C}} \quad (39)$$

$$C = 420 \text{ nF} \approx \mathbf{470 \text{ nF}} \quad (40)$$

The principle of filter attenuation is based on impedance mismatch between input and output ports. To obtain maximum attenuation the pair of 470 μH inductors, whose impedance rising with frequency, is placed near the driver input whose impedance is deemed low due to shunt capacitor after the diode rectifier. On the other hand, the 470 nF capacitor, whose impedance decreasing with frequency, is shunted near the mains side whose impedance is considered high. In CE measurement, the mains impedance would be 100 Ω , which is the LISN impedance seen by DM noise.

For technical reasons, accurate CM noise profile is not obtainable. Also, the impedance looking into the driver's line input, which acts as CM noise source, is usually large but unknown. Furthermore, since the driver is designed to be not connected to protective earth, Y-capacitors are not used in the mains EMI filter. Whereas the Y-capacitors perform the function of shunting the large output impedance of CM noise source. Those circumstances lead to difficulties in analytically determining the CM filter values. Therefore, the value of CM choke is taken by experimental trials.

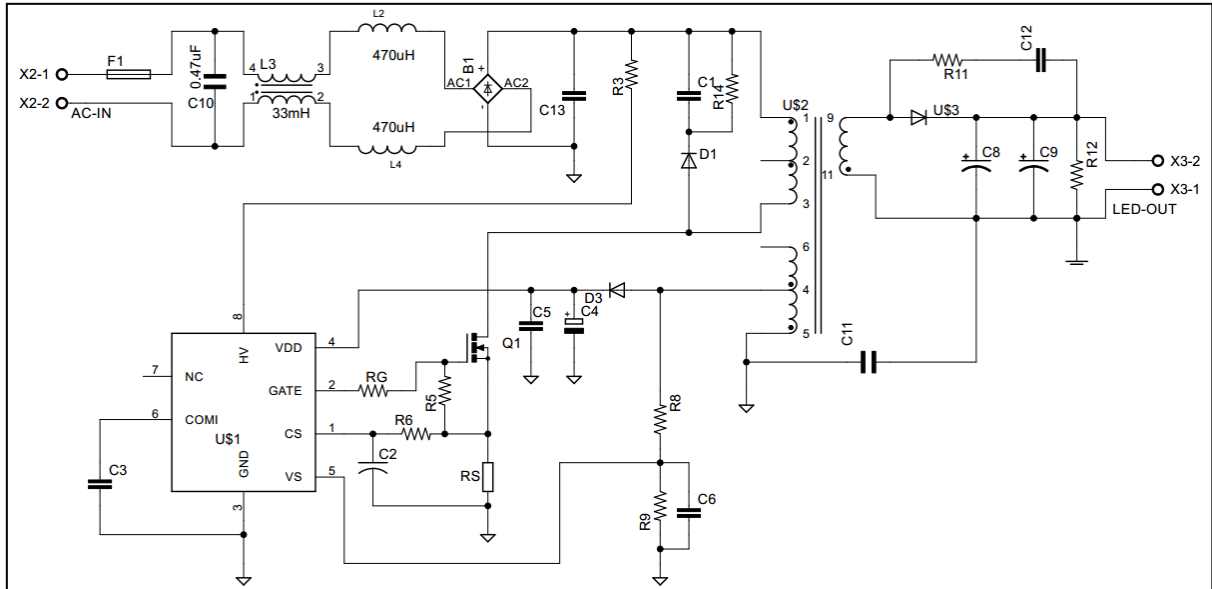


Figure 4. Schematic of the flyback LED driver

3. RESULTS AND DISCUSSION

3.1 Output Current and Voltage

Measurement shows that when R_g is 0.212Ω the actual output current is around 0.80 A, so R_g needs some adjustment. It is found that $R_s = 0.184 \Omega$ would result in output current around 1.0 A. This may be caused by the deviation of $V_{CS,PK}$ in Equation 11 and the realized primary-to-secondary turns ratio n_{PS} . Meanwhile, the range of output voltage is found to be 15.59 – 42.80 V. Figure 5 shows a constant output current with an average of 0.990 A and standard deviation of 0.012 A across the output voltage range.

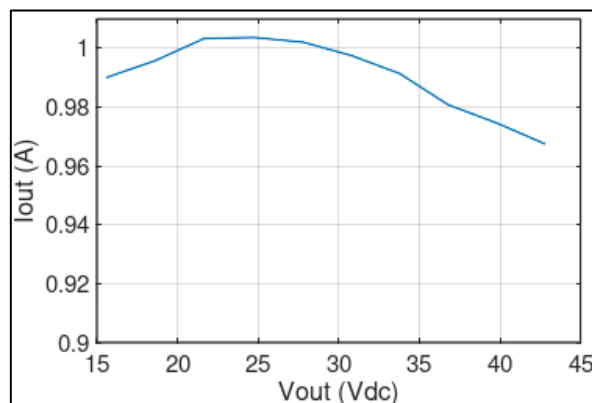


Figure 5. Output voltage and current

3.2 Power Efficiency

Power efficiency is measured in full load condition by connecting the driver output with two strings of high-power LEDs, where each string consists of a series of 14 LEDs. The output voltage and current are 43 V and 1 A, respectively. Data are taken 15 minutes after power-on, giving time for the driver to stabilize.

With a gate driving resistance R_g of 10Ω , the power efficiency reaches up to 90.35%, as shown in Figure 6. However this low R_g leads to sharp MOSFET turn-off transition, and

eventually causes significant oscillation of drain voltage. In this particular driver circuit, the oscillation produces high level of conducted emission at the high-end of frequency range, like shown in Figure 7. By experimental trials, it is found that R_g of 47Ω is sufficient to suppress the emission below the Standard limit lines. But this has reduced the power efficiency to at most 88.55%. Therefore, the choice of R_g is a trade-off between power efficiency and level of conducted emission.

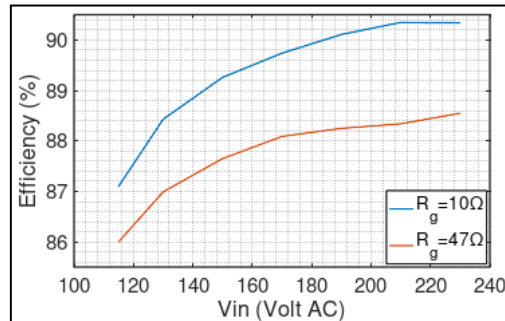


Figure 6. Power efficiency

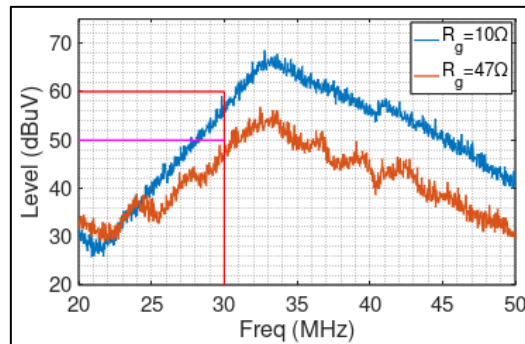


Figure 7. Effect of gate driving resistance on the conducted emission

3.3 Conducted Emissions

Figure 8 demonstrates the conducted emissions produced by the LED driver. The red and magenta lines represent the quasi-peak and average limits, respectively. The blue trace shows the measured emission when no EMI filter is in place, and it is clearly exceeding the Standard limits. On the other hand, the black trace shows the conducted emissions with EMI filter installed.

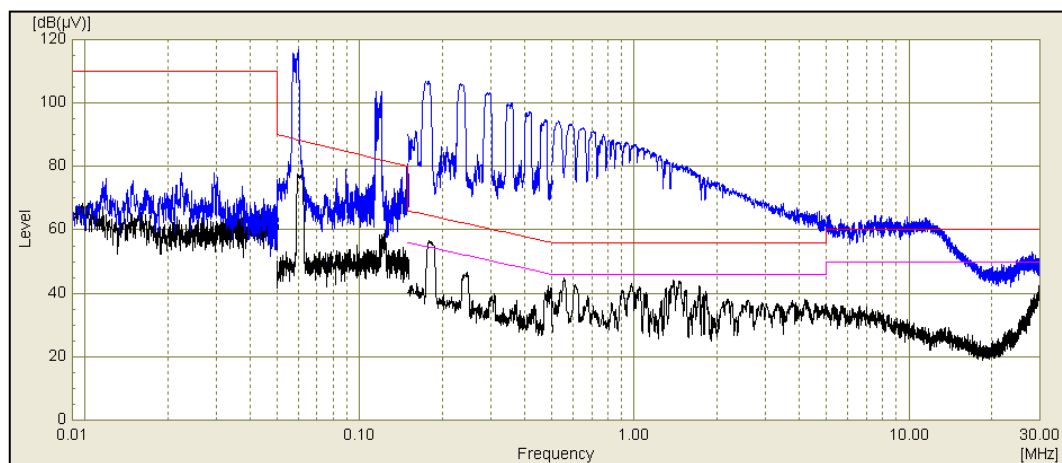


Figure 8. Comparison of unfiltered and filter conducted emission

3.4 Power Factor and Current Harmonics

Figure 9 shows the measured power factor and total harmonic distortion. The achieved power factor is 0.97-0.99. Whereas the total harmonic distortion is less than 5.22%. Figure 10 demonstrates that all the current harmonic distortions comply with the Standard IEC 61000-3-2.

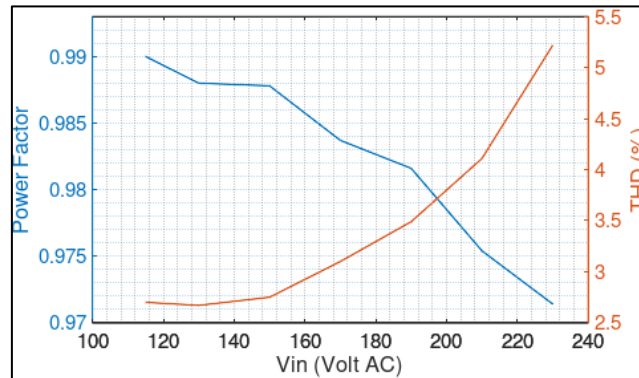


Figure 9. Power factor

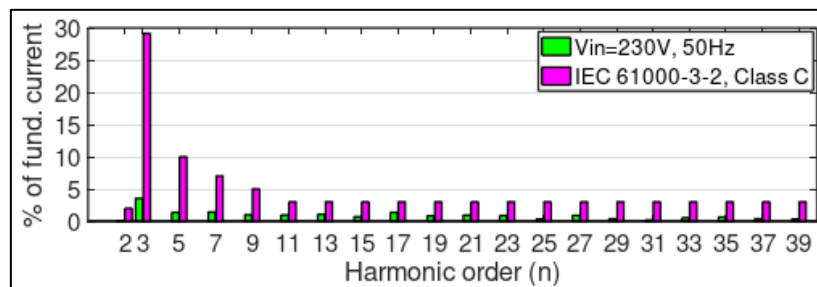


Figure 10. Current harmonics

4. CONCLUSIONS

A prototype of AC-DC LED driver has been implemented. The driver is designed to supply a constant current, and it measures an average of $0.990A \pm 0.012A$ across the output voltage $15.59V - 42.80V$. Its efficiency peaks at 88.55%. Measurements show that the current harmonics comply with IEC 61000-3 - class C, and the conducted emission levels comply with CISPR 15.

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